REMARKS

I. Status Summary

Claims 1, 2, and 4-23 are pending in the present application. Claims 1, 7, 8-11, and 15 are amended herein. Claim 8 has been canceled. Therefore, upon entry of this Amendment, Claims 1, 2, 4-7, and 9-23 will be pending under consideration. No new matter has been introduced by the present amendment. Reconsideration of the application as amended and based on the arguments set forth herein below is respectfully requested.

Support for the amendment to Claim 1 can be found throughout the present application, particularly at page 9, lines 35-38; page 10, lines 34-36; page 11, lines 9-16; page 11, line 36, to page 12, line 36; and page 14, lines 13-22.

II. Claim Rejections Under 35 U.S.C. § 112

Claim 1 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. In particular, the Examiner stated that element (f) of Claim 1 is indefinite. (Official Action, page 2.) The Examiner stated that the phrase "via a separate bus" makes the claim indefinite because "it is not clear as to the bus being separate in relation to what, two busses between the two ports or two busses between the two ports and the data memory". (Official Action, page 2.) Applicants have amended element (f) of Claim 1 to replace the phrase "a separate interface address bus" with the phrase "an interface address bus". Further, applicants have amended element (f) of Claim 1 to recite "wherein the interface address bus is separate from the data memory

address bus". Support for this amendment to element (f) of Claim 1 can be found throughout the subject application, particularly at Figure 3. Referring to Figure 3, for example, input interface buffer **9** and output interface buffer **26** are both directly addressable by data processing unit **13** via interface address bus **24** and an independent interface address space. Interface address bus **24** is provided separate from data memory address bus **18**. For these reasons, applicants submit that it is now clear that the interface address bus and the data memory address bus are separate. It is respectfully submitted that the rejection of Claim 1 under 35 U.S.C. § 112, second paragraph, should now be withdrawn.

II. Claim Rejections Under 35 U.S.C. § 103(a)

Claims 1, 2, 4-16, and 20-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants Admitted Prior Art (hereinafter, "AAPA") in view of U.S. Patent No. 6,480,929 to Gauthier et al. (hereinafter, "Gauthier"). Claims 17-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Gauthier and further in view of U.S. Patent No. 5,400,369 to Ikemura (hereinafter, "Ikemura"). These rejections are respectfully traversed.

Claim 1 recites a high speed processor. An exemplary high speed processor **1** is shown in Figure 4 of the present application. Claim 1 also recites a data processing unit for processing data. Further, Claim 1 recites a data memory which is connected to the data processing unit via a data bus and can be addressed by the data processing unit via a data memory address bus in a data address space. Exemplary processor **1** of Figure 4 also includes a data processing unit **13**, and a data memory **20** which is

connected to data processing unit via a data memory address bus **18** in a data address space. Claim 1 also recites that the high speed processor includes at least one input interface buffer which is connected to the data bus and has the purpose of buffering input data, and includes at least one output interface buffer which is connected to the data bus and has the purpose of buffering output data. Exemplary processor **1** of Figure 4 includes an input interface buffer **9** which is connected to data bus **10** and which has the purpose of buffering input data, include an output interface buffer **26** which is connected to data bus **10** and which has the purpose of buffering output data.

Claim 1 also recites a ROM memory for storing program data, wherein the ROM memory is connected to the data processing unit via lines. Exemplary processor **1** of Figure 4 includes ROM **15** for storing program data. ROM **15** is connected to data processing unit **13** via a bus **16**. Further, Claim 1 recites that the input interface buffer and the output interface buffer are directly addressable by the data processing unit via an interface address bus in an independent interface address space. Referring to Figure 4, input interface buffer **9** and output interface buffer **26** are directly addressable by data processing unit **13** via an interface address bus **24** in an independent interface address space. Interface address bus **16** is separate from data memory address bus **18**. Element (g) of Claim 1 has been added to recite wherein user data which is not to be processed by the data processing unit (such as data processing unit **13**) is passed on by the high speed processor (such as exemplary processor **1**) from an addressed input interface buffer to an addressed output interface buffer without data processing when a

single predetermined data transfer processor command is carried out by the data processing unit.

Regarding AAPA, the Examiner refers to Figure 2 of the present application. AAPA discloses a single address bus **39** for addressing data memory **41** and ports **38** and **40**. (Application, page 2, lines 2-29, and Figure 2.) Additionally, the Examiner notes that data memory **41** and input and output ports **38** and **40** all connect to address bus **39**. (Official Action, page 3.) AAPA does not disclose that input interface buffer **9** and output interface buffer **26** of process **1** are directly addressable by data processing unit **13** via a separate interface address bus **24** in independent interface address space. On the other hand, Claim 1 in element (f) has been amended to recite that the input interface buffer and the output interface buffer is directly addressable by the data processing unit via an interface address bus in an independent interface address space. Element (f) of Claim 1 also recites that the interface address bus is separate from the data memory address bus. The processor of Figure 2 of the present application does not disclose or suggest that the input buffer ($Port_{in}$) and the output interface buffer ($Port_{out}$) are directly addressable by the data processing unit via an interface address bus in an independent interface address space wherein the interface address bus is separate from the data memory address bus, as required by Claim 1. In contrast, the input interface buffer and the output interface buffer of Figure 2 are only addressable by the common address bus for addressing the various interface buffers (Ports) and the data memory. For these reasons, applicants respectfully submit that the features recited in element (f) of Claim 1 are not disclosed or suggested by AAPA. Additionally,

AAPA offers no suggestion to modify the system disclosed therein to arrive at the presently claimed invention.

Further, regarding AAPA shown in Figure 2 of the present application, the processor of Figure 2 does not disclose or suggest wherein user data which is not to be processed by the data processing unit is passed on by the high speed processor from an addressed input interface buffer to an addressed output buffer without data processing when a single predetermined data transfer processor command is carried out by the data processing unit, as recited by element (g) of Claim 1. Referring to page 4, lines 33-38, of the present application, it is explained that the processor of Figure 2 requires four processor commands to transmit input data from an input interface buffer ($Port_{in}$) to an output interface buffer ($Port_{out}$). In contrast, element (g) of Claim 1 recites a single predetermined data transfer processor command. This feature is advantageous, for example, for facilitating data transfer with a very high data transmission rate which is not slowed by a multiplicity of processor commands.

Gauthier fails to overcome the significant shortcomings of AAPA. Gauthier is directed to a microcontroller **M** connected to a dynamic random access memory **200** or other volatile memory via a data bus (DATA) and can be addressed by microcontroller **M** via a data memory address bus (DRAM ADD) in a data address space. Further, microcontroller **M** is connected to a read only memory (ROM) **202** or other volatile memory. Microcontroller **M** controls access to DRAM **200** and ROM **202**. (Gauthier, column 4, lines 66 and 67.) DRAM **200** and ROM **202** share a data bus DATA coupled to microcontroller **M**. (Gauthier, column 4, line 67, to column 5, line 2.) Applicants note

that ROM **202** as a non-volatile type memory shares data bus (DATA) with DRAM **200**, a volatile memory, so that data for the volatile DRAM **200** and for non-volatile ROM **202** are driven at appropriate times. (Gauthier, column 6, lines 19-36.) Therefore, ROM **202** does not function to store program data. Rather, ROM **202** stores data to be processed. Applicants submit that Gauthier does not disclose or suggest input and output interface buffers which are connected to a data bus and have the purpose of buffering input and output data, respectively, as recited by elements (c) and (d) of Claim 1.

In addition, applicants respectfully submit that Gauthier does not disclose or suggest the features recited in element (f) of Claim 1. Element (f) of Claim 1 recites that the input interface buffer and the output interface buffer is directly addressable by the data processing unit via a separate interface address bus in an independent interface address space. The input and output interface buffers are recited in elements (c) and (d). Therefore, because Gauthier does not disclose or suggest the input and output interface buffers recited in elements (c) and (d) of Claim 1, Gauthier cannot disclose or suggest the features recited in element (f) of Claim 1.

Referring to Figure 2A of Gauthier, a processor is disclosed having two different address buses, i.e., a DRAM address bus (DRAM ADD) and a ROM address bus (ROM ADD) allowing a pseudo-transmission concurrency by adjusting the timing of the address and control buses for volatile DRAM **200** and non-volatile ROM **202**. (Gauthier, column 2, lines 23-26.) Referring to column 2, lines 34-42, of Gauthier, microcontroller **M** executes a data cycle to non-volatile ROM **202** of the executing access cycle to volatile DRAM **200**. Second, for example, microcontroller **M** executes an access cycle

to non-volatile ROM **202** after executing an access cycle to volatile memory **200**. Third, for example, microcontroller **M** executes an access cycle to non-volatile ROM **202** and concurrently precharge volatile DRAM **200**. Fourth, for example, microcontroller **M** executes a data cycle to volatile DRAM **200** after executing an access cycle to non-volatile ROM **202**. Therefore, Gauthier teaches that a data exchange between volatile DRAM **200** and non-volatile ROM **202** on one side and a microcontroller **M** on the other side is performed in a sequential pseudo-concurrent manner via a common data bus. Applicants respectfully submit that there is no disclosure or suggestion that DRAM **200** and ROM **202** have addresses spaces that are independent from one another. Although Gauthier describes separate address buses, the reference does not disclose or suggest independent address spaces, as required by element (f) of Claim 1.

Further, Gauthier fails to disclose or suggest the features required by element (g) of Claim 1, which recites that user data which is not to be processed by the data processing unit is passed on by the high speed processor from an addressed input interface buffer to an addressed output interface buffer without data processing when a single predetermined data transfer processor command is carried out by the data processing unit. Applicants respectfully submit that these features of element (g) are not disclosed or suggested by Gauthier. For example, data from DRAM **200** and ROM **202** of Gauthier are loaded into microcontroller **M** in a pseudo-concurrent manner, sequentially via the common data bus. Gauthier does not disclose or suggest a direct transfer of data from DRAM **200** to ROM **202** or vice versa from ROM **202** to DRAM **200** via the common data bus. The data is always loaded into microcontroller **M**. Gauthier

does not disclose or suggest bypassing microcontroller **M** in a direct data transfer from an input interface buffer to an output interface buffer without passing microcontroller **M**. In other words, data which is to be transferred will always have to pass microcontroller **M**. For these reasons, Gauthier does not disclose or suggest element (g) of Claim 1.

For the above reasons, Applicants respectfully submit that AAPA and Gauthier neither teach nor suggest the features recited by Claim 1. Therefore, it is respectfully submitted that Claim 1 and its dependent claims are not obvious in view of the cited references. Claim 8 has been canceled. Applicants, therefore, respectfully request that the rejection of Claims 1, 2, 4-16, and 20-23 under 35 U.S.C. § 103(a) be withdrawn and the claims allowed at this time.

As stated above, Claim 17-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Gauthier and further in view of Ikemura. Claims 17-19 depend from Claim 1. For the reasons presented above, Claim 1 is believed to be patentable over AAPA and Gauthier. Ikemura fails to overcome the significant shortcomings of AAPA and Gauthier.

Ikemura is directed to a frame detecting device that can recognize data formats. The frame detecting device includes a shift register **101** that receives byte-wide input data. (Ikemura, column 2, lines 64 and 65, and Figure 2.) The first fifteen bits of byte register **101** are provided in parallel form as test data B to a data scanner **102** and as intermediate data C to an aligner **104**. Ikemura, column 3, lines 2-5. Data scanner **102** searches for the value A1 in the test data B received from shift register **101** by comparing A1 with bits 1-8, with bits 2-9, etc. Ikemura, column 3, lines 6-10. Data

scanner **102** can perform these eight comparisons simultaneously and output the result as alignment data D and E. Ikemura, column 3, lines 10-13. Applicants submit that Ikemura does not disclose or suggest input and output interface buffers which are connected to a data bus and have the purpose of buffering input and output data, respectively, as recited by elements (c) and (d) of Claim 1. In addition, Ikemura does not disclose or suggest the additional features of the input and output interface buffers as recited in element (f) of Claim 1. Further, Ikemura does not disclose or suggest the features recited in element (g) of Claim 1. Accordingly, Claim 1 is believed to be patentably distinguished over the combination of AAPA, Gauthier, and Ikemura.

Because Claims 17-19 depend from Claim 1, the comments presented above relating to Claim 1 apply equally to Claims 17-19. Thus, Claims 17-19 are believed to be patentably distinguished over AAPA, Gauthier, and Ikemura. Applicants respectfully request that the rejection of Claims 17-19 under 35 U.S.C. § 103(a) be withdrawn and the claims allowed at this time.

III. Conclusion

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and such action is earnestly solicited.

If any minor issues should remain outstanding after the Examiner has had an opportunity to study the Amendment and Remarks, it is respectfully requested that the Examiner telephone the undersigned attorney so that all such matters may be resolved

and the application placed in condition for allowance without the necessity for another Action and/or Amendment.

DEPOSIT ACCOUNT

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

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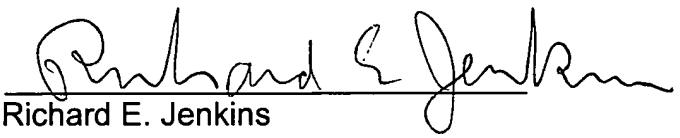
Date: June 2, 2005 By: 

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